Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **ADJ**
2. **N/C**
3. **OUTPUT**
4. **V IN**
5. **OUTPUT**
6. **OUTPUT**
7. **V IN**

**C**

**3 5**

**7**

**4**

**1 6**

**MASK**

**REF**

**.093”**

**.096”**

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: .004” X .004”**

**Backside Potential: OUTPUT**

**Mask Ref: C**

**APPROVED BY: DK DIE SIZE .093” X .096” DATE: 9/22/21**

**MFG: NATIONAL THICKNESS .010” P/N: LM150**

**DG 10.1.2**

#### Rev B, 7/1